AMENDMENTS

In the Specification:

Please amend the paragraph beginning at page 1, line 8 as follows:

A1

A conventional memory address extension device includes a register bank in every task. The register bank consists of a plurality of page registers which are combined therewith. The page register stores therein CPU (central processing unit) address and upward address of extended address which is broader than the CPU address. When task ~~switch~~ switching occurs, the memory address extension device extends memory address space ~~in such a way of causing~~ so as to cause the register bank to be switched.

Please amend the paragraph beginning at page 1, line 15 as follows:

A2

However, ~~in~~ the conventional technique described above[[,]] ~~on the supposition~~ presupposes that there exists a data to which only a certain task may ~~accesses~~ access. However, another task may be capable of accessing ~~such the~~ data to which only the determined certain task should access. Therefore, there is the problem that the data which should only be accessed by the determined certain task is capable of being rewritten wrongly by the another task.

Please amend the paragraph beginning at page 2, line 26 as follows:

A3

According to a third aspect of the present invention, in the first aspect, there is provided a memory address space extension device, wherein, as to the definition table, it causes combination that access is permissible or ~~in-permissible~~ impermissible with respect to read and / or write to the data area respectively to be defined.

Please amend the paragraph beginning at page 11, line 6 as follows:

A4

According to such procedure, it is capable of preventing data area from ~~wrongly accessing~~ impermissibly being accessed by ~~the~~ a task which is not permitted ~~the~~ access. Consequently, it is capable of protecting the data from being accessed ~~accessing~~ wrongly by the task which is not permitted accessing thereto.

Please amend the paragraph beginning at page 11, line 10 as follows:

A5

Next, there will be described operation of the present embodiment ~~while~~ using a concrete example.

Please amend the paragraph beginning at page 12, line 19 as follows:

A6

In the first embodiment, the access right of the data area access right definition table 11 of Fig. 4 is only "permissible" or ~~"in-permissible"~~ "impermissible". However, in

A6 the present embodiment, as shown in Fig.6, there are four kinds of ~~the~~ access right of the data area access right definition table 11. The four kinds of ~~the~~ access rights are "readable, in-writable", "in-readable, writable", "readable, writable", and "in-readable, in-writable". These points are different from the first embodiment.

Please amend the paragraph beginning at page 19, line 18 as follows:

A7 As described above according to the present invention, there is provided the table of defining that the access right is permissible or the access right is ~~in-permissible~~ impermissible by the task with respect to certain data area. Thus, it is capable of preventing wrong access from the task with respect to a certain data area. For that reason, it is capable of protecting the data of the area, thus, it is capable of improving the reliability of the data.

Please amend the paragraph beginning at page 19, line 24 as follows:

A8 Further, according to the present invention, there is provided ~~the~~ a table ~~of~~ defining ~~that~~ whether the access right is permissible or the access right is ~~in-permissible~~ impermissible by the task with respect to a certain data area or the interruption processing. Thus, it is capable of preventing wrong access from the task with respect to a certain data area and / or the interruption processing. For that reason, it is capable of protecting the data of the area, thus, it is capable of improving the reliability of the data.

Please amend the paragraph beginning at page 20, line 1 as follows:

Furthermore, in the above described definition table, it causes combination that

A9 the read, and the write with respect to the data area are permissible or ~~in permissible~~ impermissible respectively to be defined, thus it is capable of executing fine-grained control in answer to the inputted CPU data.